16-CHANNEL NEURO PRE-CONDITIONER DEVICE

J. Morizio[1], D. Won[2], I. Obeid[2], C. Bossetti[2], M. Nicolelis[3], P. Wolf[2]
[1]Department of Electrical and Computer Engineering, Duke University, NC, USA
[2]Department of BioMedical Engineering, Duke University, NC, USA
[3]Department of Neuroscience, Duke University Medical Center, NC, USA

Abstract- **In this paper we present the mixed-signal circuit design, layout, implementation techniques, and test data for a 16-channel neuro pre-conditioner device that is used to amplify and filter neuron spike signals acquired from chronically implanted electrodes of an animal's brain. Schematics and simulation data for each of the sub-circuit macros are presented which include a high gain, continuous time 1st order bandpass filter pre-amplifier, a cascaded bandpass switch capacitor filter, a selectable gain output buffer, and a VCO sourced clock generation circuitry. This device was implemented using AMI's, 0.5um, double poly, triple level metal CMOS technology. The device layout and floorplan, specifications and test data conclude this paper.**

Keywords **- Application Specific Integrated Circuit (ASIC), Analog Signal Processing, Neuron Preconditioning**

I. INTRODUCTION

Neuron signals source from electrodes implanted in a animal's brain require analog signal processing or signal preconditioning prior to the A/D conversion and spike sorting algorithms used in a neuron data acquisition system [1,2,3]. Gain above of 80dB, bandpass filtering above 4th order and input referred noise below 4µv rms are stringent specifications of the signal preconditioning electronics. Integration and packaging of these multi-channel analog functions into a lightweight, miniaturized package located physically close to the electrodes is also desirable. It is for the above reasons a neuron preconditioning analog ASIC was developed with the floorplan shown below:

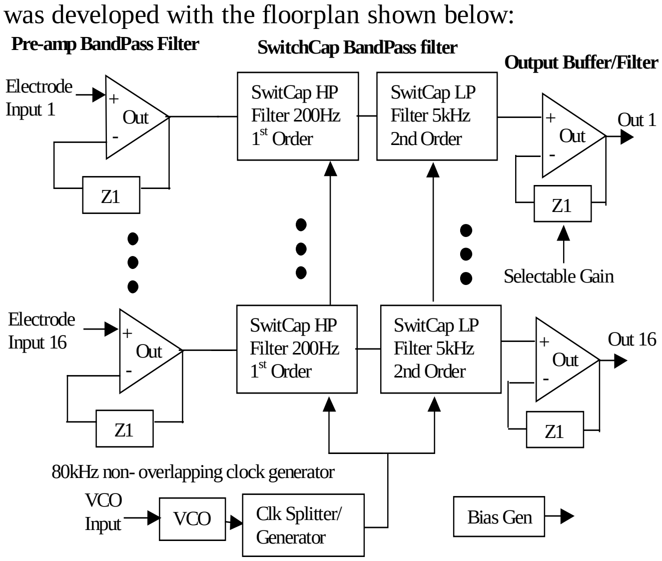

Fig. 1. Sixteen Channel Neuro Preconditioner ASIC floorplan.

Each analog channel has a low noise, high gain bandpass preamplifier followed by cascaded highpass and lowpass switch capacitor filters. The final output amplifier stage will amplify and drive the switch capacitor filter output off-chip.

II. CIRCUIT DESIGN

A. Pre-amplifier Circuit

The preamplifier circuit actually interfaces to the implanted electrodes chronically implanted in the brain. Hence, it is critical that this circuit have large input impedance above 5M ohms, output impedance below 300 ohms to drive the switch capacitor filter input stage, moderate signal gain above ten, low input referred noise below 4us rms, and signal offset of less than 20mV[4]. The circuit design and gain response is shown below:

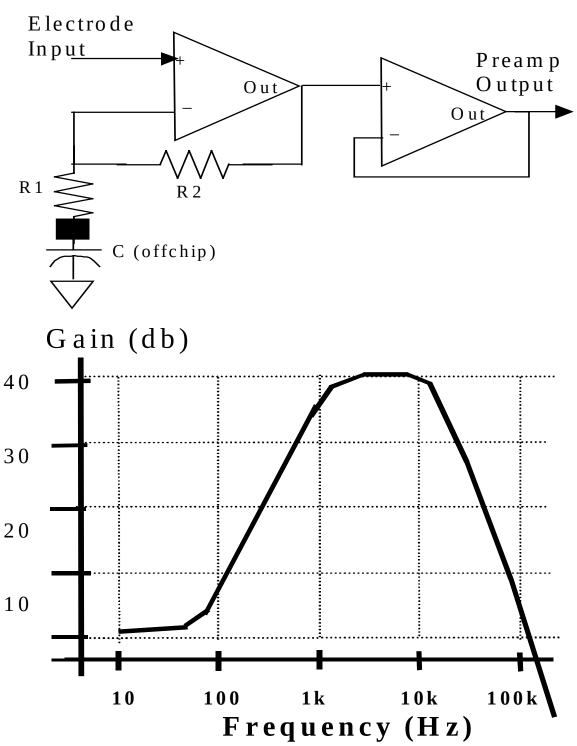

Fig. 2. Preamplifier Circuit.

The preamplifier consists of a bandpass filter cascaded by a source follower. The continuous time bandpass filter circuit includes one off-chip capacitor, two internal resistors and two operational amplifiers (Opamp). At DC the gain is unity of one. A high pass zero location is set by the R1*C product. The bandpass gain is set by (R2/R1) + 1. The low pass pole location is set by the gain (G) and bandwidth (BW) product of the operational amplifier. The Laplacean transfer function of this preamplifier circuit is below:

$$V_{OUT}/V_{IN}(s) = [(R_2/(R_1+1/Cs))+1][1/(s+G*BW)] \qquad \text{Eq.1}$$

The preamplifier was designed to have an input impedance of 8M ohms at 1Khz, an output impedance is 250 ohms, passband gain of 43dB, input referred noise of 3.5µv rms and signal offset of less than 20mv.

B. Bandpass Switch Capacitor Filter

Additional cascaded filtering is needed to increase the order of bandpass filtering of the analog channel beyond the first order pre-amplifier bandpass stage. Third or fourth order bandpass filtering is desirable to remove noise outside the neuron pulse bandwidth which is between 500Hz to 8kHz [5]. Due to the integration and packaging constraints of this device, it is also important to minimize all off-chip passive components for this bandpass filter stage. Hence, either G_mC or switch capacitor filters architectures are needed. The switch capacitor architecture was selected the over G_mC because it allowed for filter bandwidth adjustments by the use changing clock frequency. To achieve the passband frequency of 500hz to 8Khz, highpass filter is cascaded by a low pass filter below:

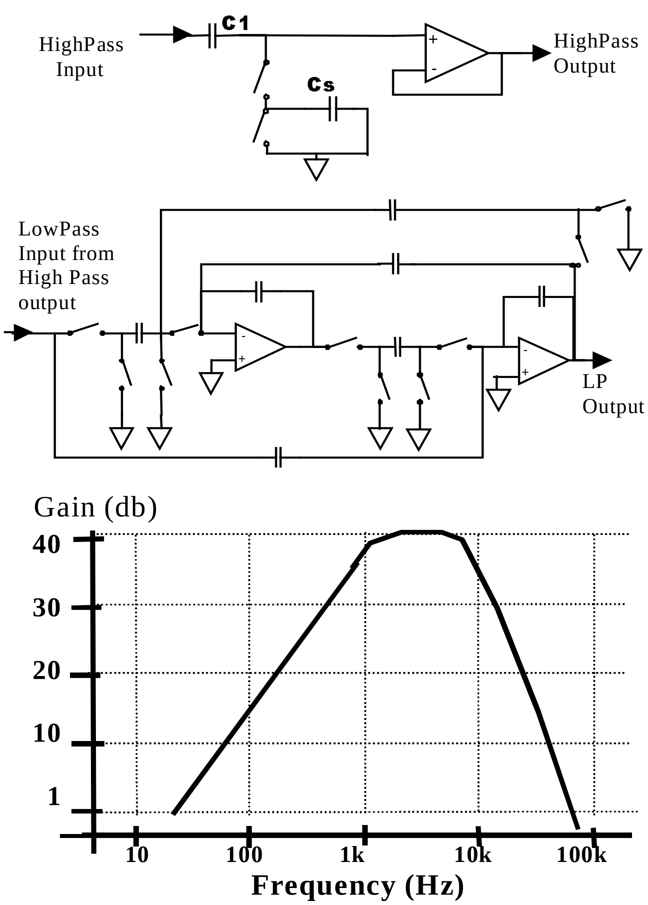

Fig. 3. Bandpass Switch Capacitor filter and Gain Response

The switch capacitor bandpass filter uses two non-overlapping 80kHz clocks which are generated from the VCO and clock generator macro.

The s-domain and z-domain transfer function of the highpass filter are below in Eq. 2 and Eq. 3 respectively:

$$HP(s) = s / [s + C/(Cs * f_{clk})] \qquad \text{Eq. 2}$$

where: C = 12pF, Cs = 0.5pF and f_{clk} is 80Khz

$$HP(z) = z + 1 / [(z + 1) + (C(z-1)/(Cs * f_{clk}))] \qquad \text{Eq. 3}$$

The s-domain and z-domain transfer functions of the 2nd order BiQuad LowPass Filter are below in Eq. 4 and Eq.5 respectively:

$$LP(s) = 9.87e8/(s^2 + 4.44*10^4 s + 9.87*10^8) \qquad \text{Eq. 4}$$

$$LP(z) = 0.3948 (z^2 + 2z + 1) /(6.17z^2 – 7.21z + 2.62) \qquad \text{Eq. 5}$$

Mixed signal layout techniques are critical to the size and accuracy of the switch capacitor filter. These techniques are discussed in detail in Section III of this paper.

C. Output Driver Amplifier

The last stage of the analog channel is the final amplifier stage of the analog channel in the precondition device. This amplifier circuit can drive the filtered neuron pulses off-chip into a large capacitive load of 100nF. It was decided to put a selectable gain control on this amplifier stage to offer a gain variable for the neuroscientist.

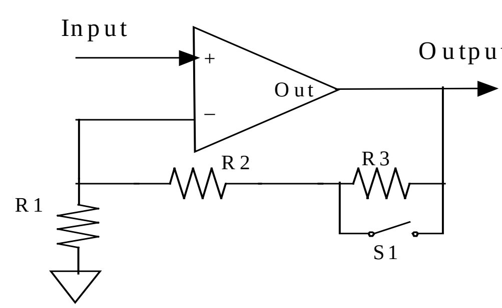

Fig. 4. Preamplifier Circuit.

The DC gain equations for this amplifier ignoring the S1 switch resistance are:

$$V_{OUT}/V_{IN} = [(R_2 /R_1) + 1 \qquad \text{for S1 closed} \qquad \text{Eq. 5}$$
$$V_{OUT}/V_{IN} = [(R_2 + R_3 /R_1) + 1 \qquad \text{for S1 open} \qquad \text{Eq. 6}$$

The output amplifier stage that we implemented had a low gain setting of 10 and a high gain setting of 40. Another benefit of this amplifier stage is that it acts as a lowpass filter which will reduce some of the transient noise caused by the switch capacitor clock edges.

D. Voltage Controlled Oscillator

The 31-stage voltage controlled oscillator (VCO) uses a current starved delay cell. The frequency is controlled by an off-chip bias voltage. The VCO gain was selected to have a center frequency of 5.12Mhz so that when divided by 64 will produce a 80kHz clock which is needed for the switch capacitor filters. The VCO topology and simulation results are shown below:

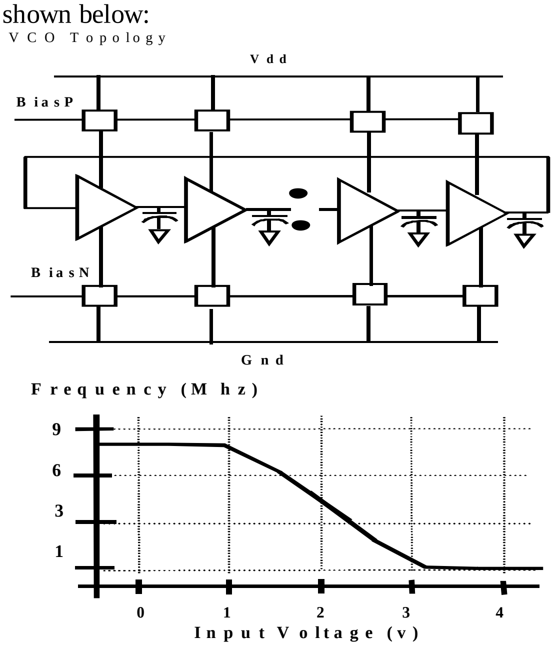

Fig. 5. VCO topology and Frequency Gain Curve

The normal operation of the VCO input is 1.8v.

III. CIRCUIT LAYOUT AND DEVICE FLOORPLAN

Classic mixed-signal circuit layout techniques were used to implement the floorplan of this preconditioner ASIC[7]. Separate Vdd and Gnd power routing and pads were used to isolate the digital and VCO logic with the analog amplifiers. Mixed-signal n+ and p+ diffusion guard rings were placed n the periphery of all analog and digital circuits to isolate the substrate. Within all of the open areas inside of the ASIC, power supply decoupling capacitors was placed to reduce Vdd and Gnd bouncing.

Shown below is a layout of the switch capacitor filters showing the common centroid capacitors and Opamp floorplan:

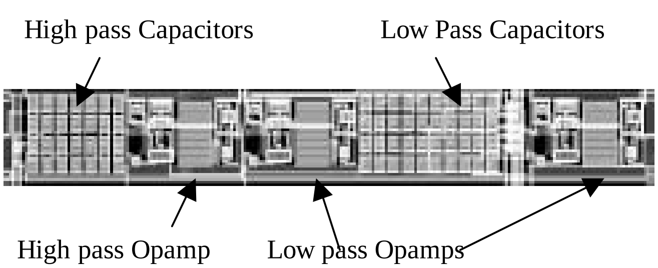

Fig. 6. Switch Capacitor Filter

The switch capacitor filter unit size capacitor is .5pF and is poly-poly type to minimize the voltage coefficients. This value was selected to yield the best area, noise and matching characteristics [8]. The critical dimension of the filter layout is the height dimension of 160μm which matches the pad pitch of precondition device.

The 16 channel preconditioner die size is 3.8mm x 4.2mm and is shown below:

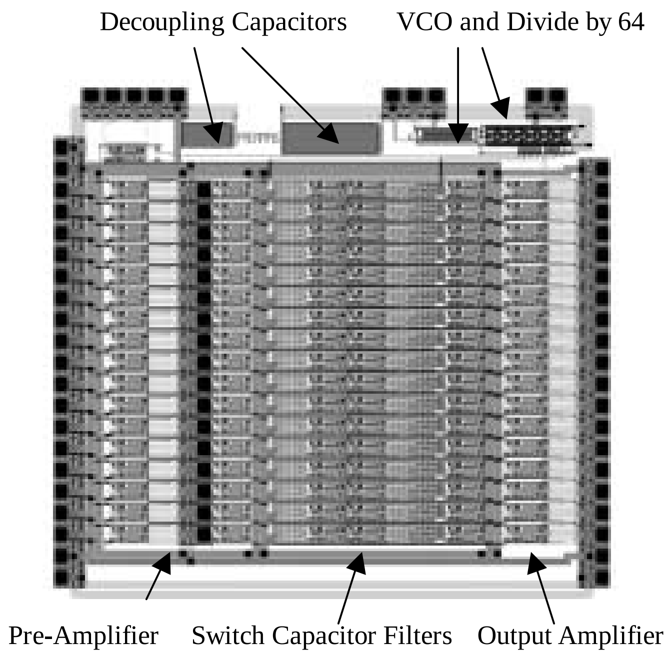

Fig. 7. Full chip plot

The die floorplan matches that of ASIC floorplan in Fig. 1. The input pads are on the left side and the output pads are on the right side with each channel having a preamplifier, switch capacitor filters and output amplifier.

IV. TEST RESULTS

This device was fabricated using the AMI's, 0.5um, double poly, triple level metal CMOS technology. The preconditioner ASIC evice was fabricated and packaged in a 181 pin PGA package. A printed circuit board (PCB) was designed and fabricated to test the preconditioner ASIC. This PCB test board is shown below:

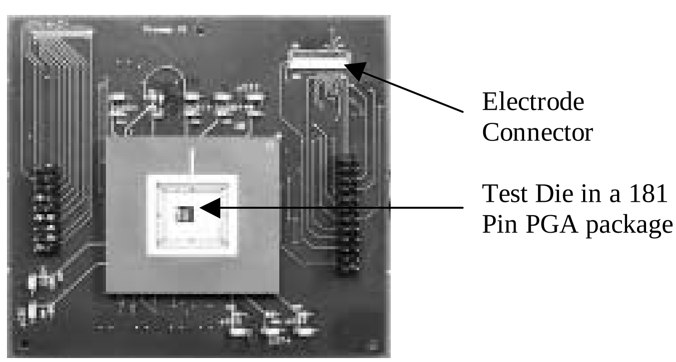

Fig. 8. PCB Test Board

The Bionic Technologies neural signal simulator was used to test the preconditioner ASIC using a 250μv peak to peak input with 220k ohms output impedance. Below are output waveforms of the ASIC at low gain setting with a mvolt scale indicating a gain of 61db.

mVolts scale output levels

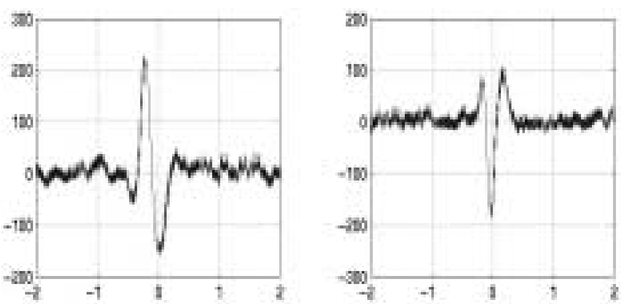

Fig. 9. Analog Output waveforms from 250 μv input

The preconditioner test device was characterized by using the the following tests with data was collected accordingly presented in Table 1:

TABLE 1. Measured Test Data

Test Measurement	Data	Notes
Gain @1kHz	73 dB 61 dB	For High Gain For Low Gain
Input Impedance	12M ohms	At 1kHz input signal
Output Impedance	210 ohms	At 1kHz signal
Channel CrossTalk	< -48db	Less than for adjacent channels
Output Slew Rate	+5v/us -4v/us	Pos. SR for 1uF Neg. SR for 1uF
Input Voltage Range	1.8mv .21mv	Low Gain High Gain
Offset Error	20mv	
Power Consumption	148 mw	For 5v power supply
Input Referred Noise	3.8μvrms	For 400hz – 22Khz

V. CONCLUSION

In this paper we presented the circuit design, layout and test data for a 16-channel neuron ASIC that will be used for neuron signal preconditioning. Schematics, simulation data, and layout for each of the sub-circuit macros were presented. This ASIC device does function as specified and can be used to amplify and filter neuron spike signal acquired from chronically implanted electrodes of an animal's brain. However, additional gain of +10dB and another order of filtering is actually needed to accommodate all of the preconditioning requirements for a DAQ system [1] to perform spike sorting. This is not problem since most of the DAQ systems such as Plexon's MAP Boxes have this capability anyways.

Our future plan in 2003 is to package two of these devices into a flip-chip tethered 32-Channel headstage sub-assembly and use sub-assembly on a living monkey or rat. This 10mm x 13mm tethered headstage sub-assembly will be located right near the brain electrode connectors**.**

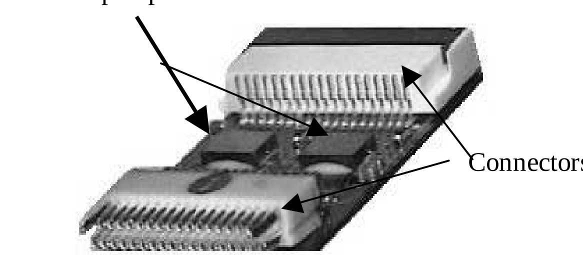

Fig.10. Headstage Sub-Assembly 10mm x 10mm

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