A MULTICHANNEL CMOS ANALOG FRONT END IC FOR NEURAL RECORDINGS

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Abstract- **A multichannel integrated circuit for processing extracellular neural signals has been designed and manufactured. The analog CMOS IC consists of 17 parallel channels, each comprised of three cascaded stages: bandpass filter with gain, switched capacitor filters, and output buffer with selectable gain. The bandpass filter stage features an opamp with non-inverting resistor feedback and an off-chip capacitor in the feedback pathway to provide gain (43dB) and one high pass filter pole (220Hz). The low pass pole is set by the gain-bandwidth product of the opamp. In the switched capacitor filter stage, a one-pole high pass filter (500Hz) cascades into a two-pole biquadratic low pass filter (5kHz). The switched capacitor filters may be controlled by either an on-board tunable ring oscillator centered at 50kHz or an off-chip clock. A four-phase clock splitter provides the necessary filter control-signals; a phase delay of 180° between the high and low pass clock lines maximizes settling time between the filters. The output buffer stage provides selectable gain at 20dB or 32dB. The IC was manufactured by AMI using a 0.5μm triple metal double poly process, and measures 4.2 x 3.8mm. The die is designed to be packaged in a flip-chip sub-assembly.**

Keywords **- Neural prosthetics, neurochip, multichannel neural IC**

I. INTRODUCTION

The development of hybrid brain-machine interfaces will require new instrumentation technology for neural signal acquisition and processing. Integrated circuits (IC) must be developed for wireless, high-density, multi-electrode processing [1]. We are currently developing a series of preamplifier headstages based on custom analog CMOS ICs [2]-[5]. The ICs are designed around typical neural signal constraints such as large low-frequency offset voltages, small signal amplitudes, and low signal to noise ratios [5], [6]. In this paper, we present a multichannel analog IC that applies two high pass (530Hz) and two low pass (5.3kHz) filter poles with a selectable gain of 61 or 73dB.

II. SYSTEM DESIGN

We have designed and manufactured a multichannel analog neural preamplifier. The device consists of 17 parallel channels – 16 for neural signals plus one for a reference electrode signal. It is designed to interface directly to implanted cortical microwire electrodes and to output to a commercial neural signal acquisition unit via a cable tether. The channel block diagram is shown in Fig. 1. Each channel consists of a bandpass filter stage, a switched capacitor filter stage, and an output stage with selectable gain. This design provides high input impedance combined with high pass filtering in the first stage to prevent electrode loading and to reject electrode offset voltages. The subsequent stages reject out-of-band noise and apply more gain before driving the signal at the output.

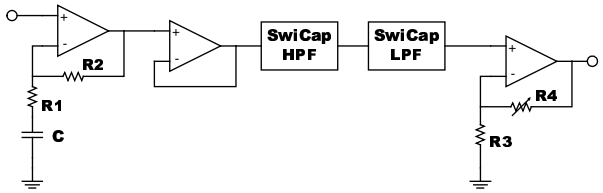

Fig. 1. Channel block diagram. Each channel is comprised of a bandpass filter input stage, a switched capacitor filter stage, and an output stage with variable gain. Note that capacitor C is located off-chip.

The bandpass filter stage is based on two opamps. The first uses resistors and a capacitor in the non-inverting feedback path to generate a single high pass filter pole with gain. Although the capacitor C must be placed off-chip due to the prohibitive size of capacitors in silicon ($950 \cdot 10^{-18} F/\mu m^2$), this architecture requires only one I/O per channel to do so. The gain and high pass filter pole are determined by the equations $A_1 = 20\log_{10}(1 + R_2/R_1)$ and $f_{-3dB} = 1/2\pi R_1 C$. Using the device values in Table I, these are predicted to be 43dB and 220Hz, respectively. The low pass filter pole of the bandpass filter, determined by the gain-bandwidth product of the opamp, is predicted at 15kHz. An opamp in source follower configuration is placed at the output of the bandpass filter in order to properly drive the switched capacitor filter stage.

The switched capacitor filter stage implements a unity gain bandpass filter (500Hz – 5kHz) to further attenuate out-of-band noise and low frequency offset voltages. Switched capacitors are not applicable in the first (input) stage because of the risk of corrupting the unamplified neural signals with switching noise and the need for anti-aliasing in a prior stage. The bandpass filter is implemented as a single pole high pass filter cascaded with a biquadratic low pass filter. These filters are based on a previous design which was successfully manufactured and tested using external clock signals [7]. The filters in this IC are controlled by a master clock signal generated by an on-board tunable ring oscillator (VCO). The VCO output is centered at 3.2MHz and drives a divide-by-64 circuit whose output feeds a clock splitter. The resulting four non-overlapping clock phases directly control the high pass filter switches and are then phased by 180° (using an inverter buffer chain) to control the low pass filter switches.

The output stage consists of an opamp configured as a non-inverting amplifier with selectable gain. The gain, determined by the equation $A = 1 + R_4/R_3$, is made selectable by using two series resistors for R_4, one of which

TABLE I
PASSIVE DEVICE VALUES IN THE PREAMPLIFIER INTEGRATED CIRCUIT

Device	Value
R_1	7.33kΩ
R_2	1.008MΩ
R_3	20kΩ
R_4	160kΩ (+ 640kΩ)
C	100nF

can be shorted using a CMOS pass-gate. Using the resistor values listed in Table I, the gain was designed to be either 20dB or 32dB. This gives the channel an overall gain of 61dB or 73dB, enough to amplify neural signals in the range of 100's of microvolts. The output stage will also exhibit a low pass characteristic (~20kHz), determined by the opamp gain bandwidth product, which will help smooth clock noise from the switched capacitor filter stage.

The opamps used in this device are based on a previously tested three-stage design. The opamps have an n-type input differential pair stage, a gain stage, and an output buffer stage. Simulations predicted an open loop gain of 51.1dB, a phase margin of 132°, and a gain bandwidth product of approximately 2MHz. The opamp noise density is $27.7nV/\sqrt{Hz}$.

III. RESULTS

The device was laid out using Mentor design tools and manufactured using the AMI 0.5µm triple metal, double poly process. Sensitive opamp structures were protected from substrate noise with guard rings, while centroid layout techniques were used to preserve resistor and capacitor ratios. Switching signals were isolated from analog signals to prevent interference. All switches were placed together in each switched capacitor filter and buffered with guard rings. The overall layout area was 4.2 x 3.8mm. The layout required 68 I/Os, including 17 each for inputs, outputs, filter off-chip capacitors, and six each for V_{DD} and V_{SS}. The off-chip capacitor I/Os were placed in the layout's interior to simplify routing. The die is therefore well suited to be flip-chip mounted onto a sub-assembly package, which will save area and increase packing density over standard IC packaging solutions.

The preamplifier headstage is powered via three cables providing V_{DD} = 2.5V, V_{SS} = -2.5V and ground, with the ground used as the reference voltage for all of the opamp feedback loops. During in vivo recordings, the ground rail must be attached to a neutral reference wire on the subject in order to ground the subject and prevent offset saturation. Separate V_{DD} and V_{SS} power busses are used for the analog and digital sections of the chip. This helps prevent clock switching noise from deteriorating the analog signals via the power busses.

TABLE II
SUMMARY OF SIMULATION RESULTS

Stage	Gain (dB)	f-3dB (Hz)	Rolloff (dB/dec)
Input (BPF)	43	220, 15k	-20, -20
SwiCap HPF	-1.8	501	-19
SwiCap LPF	-0.06	5.3k	-35.8
Output	20, 32	~20k	-20

Each section of the circuit was simulated extensively using Avanti HSPICE prior to fabrication. A summary of the simulation results is seen in Table II. Due to the relative robustness of the opamp, the input (bandpass filter) and output stages simulated as expected. The sampled discrete-time nature of switched capacitor filters prevented AC HSPICE analysis from being used to obtain the frequency response. Instead, sinusoidal inputs were swept across frequencies from 100Hz to 10kHz under transient analysis. The output amplitudes were measured and gain was plotted versus frequency to obtain the simulated output frequency response.

IV. CONCLUSION

A multichannel analog CMOS preamplifier has been designed, manufactured, and is being tested. The device includes gain and filtering to process electrode derived neural signals in a densely packed form factor close to the brain.

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