Design and Implementation of Switched-Capacitor Filters for an Integrated NeuroChip

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Abstract

An implantable integrated circuit which records and processes neural signals requires an on-chip bandpass filter. Single-pole high and low-pass stages in basic non-inverting and follower (HP1N, HP1F, LP1N, LP1F) configurations were designed and simulated using HSPICE. Sallen-Key and standard biquadratic SC high- and low-pass filters (SKLP, SKHP, LPBQ, HPBQ) were likewise designed and simulated. Based on simulation results, the HP1F, LP1N, SKLP, and LPBQ stages were built using common centroid capacitor techniques in the MOSIS AMI 0.5μm CMOS process. The fabricated filters were tested using AudioPrecision and the frequency response was accurate to within 5%. The HP1F-LPBQ cascade would add approximately 0.23 mm^2 to each channel of an existing neurochip prototype.

1 Background

Performing real-time processing of neural signals from freely-behaving animals requires an implantable integrated circuit (IC) chip. Such a chip would allow electrical signals from the brain to be acquired and processed and for the output control signals to be transmitted through RF telemetry to some external prosthetic device. The raw signals acquired by the neuro-chip from the recording electrodes will be contaminated by both high frequency electrical noise as well as low frequency noise from unwanted activity of the animal, such as breathing and chewing. To condition neural spikes, the passband should extend from approximately 500 Hz to 5 kHz.

Traditional bandpass filters in this frequency range require resistors and capacitors too large to be integrated onto a high-density channel implantable neural recording chip. Switched capacitors can be used to implement the filters economically and accurately in the neurochip. A switched capacitor is a capacitor of value C that is connected to different voltage nodes on alternate halves of the switching period and acts analogously to a resistor of value $\frac{1}{fC}$, where f is the switching frequency. Thus, switched capacitors can reduce the area of the filter enough to be implemented on a chip that can be implanted in the brain. For example, a capacitor switched at a clock frequency of 50kHz would consume 96% less area than its equivalent resistor (using squares of $3L_{min}^2$) even with a high-resistivity mask.

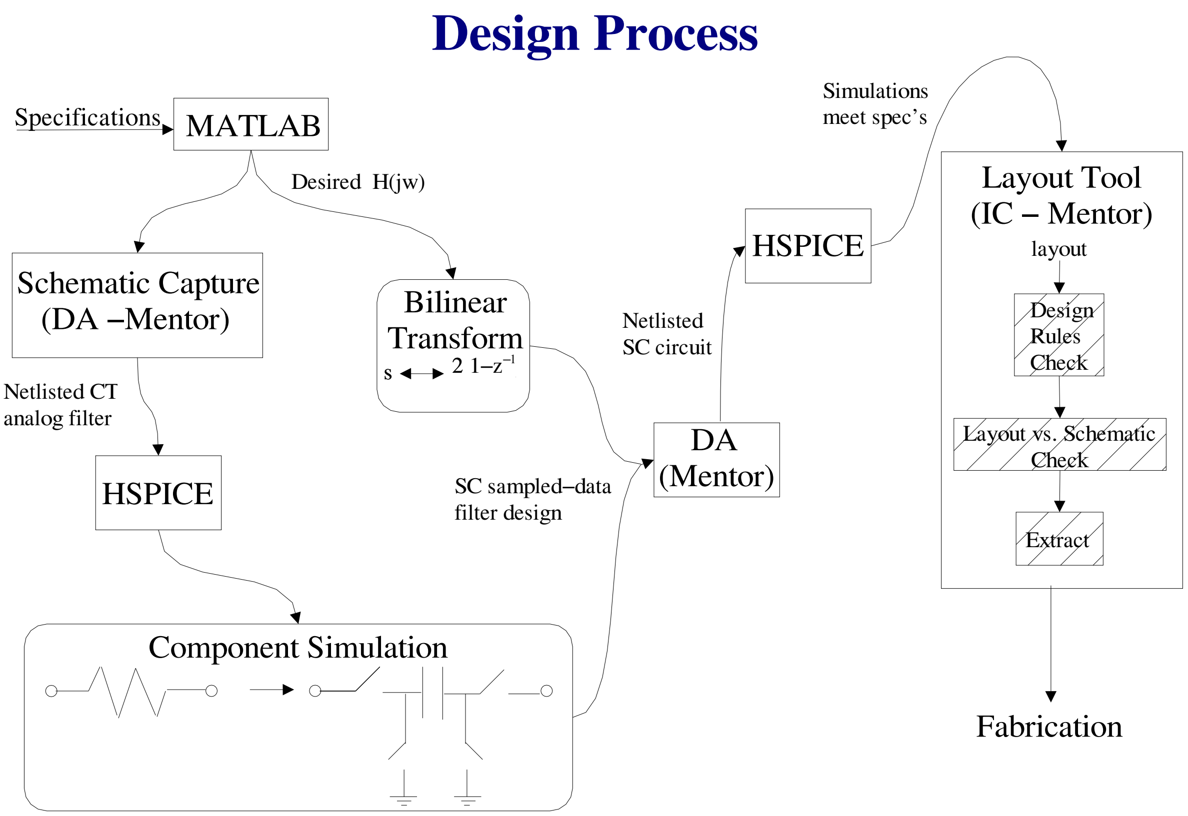

Figure 1: Design flow

2 Design

2.1 Procedures

The design phase consists of several steps to get from the input specifications to layout and fabrication and employs several different software and hardware design and analysis tools, as illustrated in figure 1.

Target transfer functions were determined from the specifications on the frequency response: unity-gain, passband from 500 Hz to 5 kHz, -40dB/dec low-pass attenuation, and -20dB/dec high-pass attenuation. Designing the filter in stages that could be cascaded to meet these criteria was chosen over one low-Q bandpass filter due to relative flexibility and ease of design. Design attempts were made at both high-pass and low-pass filters in the following configurations:

- 1st-order non-inverting (HP1N, LP1N)
- 1st-order follower (HP1F, LP1F)
- 2nd-order Sallen-Key (SKHP, SKLP)

- 2nd-order standard SC biquadratic (HPBQ, LPBQ)

Component values were calculated to match the transfer function of the actual filter to the desired transfer function, and bode plots of both the desired and expected transfer functions were compared in Matlab. The CT filter schematics were drawn up in Mentor's schematic capture tool DA. Once functionality was verified with AC analysis in HSPICE, the resistors were replaced with switched-capactors (SC). With the exception of HPBQ and LPBQ, component simulation was used to convert the RC continuous-time filters into their SC counterparts. For the Sallen-Key configurations, different quality factor (Q) values were tested before deciding on the maximally flat response at Q=0.707. For the SC biquadratic filters, taken from [1], bilinear transformation was carried out on the target transfer function to match the given circuit transfer function.

These schematics were once again netlisted and the simulated in HSPICE. Due to the sampled discrete-time nature of SC filters, AC analysis could not be performed to obtain the frequency response. Instead, sinusoidal inputs were swept across frequencies from 100Hz to 10kHz under transient analysis. The output amplitudes were manually measured and gain plotted versus frequency to obtain the simulated output frequency response. As desired results were obtained, simulations were modified to model more closely the actual realization of the filter; for example, by changing the ideal voltage sources for the four clock signals to outputs of the clock generator subcircuit.

2.2 Schematics and Layout

The filters that were chosen for implementation based on how well simulation outputs met specifications were HP1F, LP1N, SKLP, and LPBQ. The schematics taken directly from DA are shown in figure 2. All filters were implemented with a stray-insensitive design.

All four filters were layed out using Mentor's IC tools in the 0.5μm double poly triple metal CMOS process. Poly-electrode capacitors were used and arrayed in a centroided arrangement. Care was taken to keep switching signals from interfering with analog signals. With the exception of the standard biquadratic low-pass filter, the CMOS transmission gate switches for each filter were separated from the op-amps by the capacitor arrays. All switches were kept together in each filter and buffered with guard rings. Op-amps and a 4-phase clock generator, which have been fabricated and tested previously [2], were simply instantiated as cells. The layout of each stage was catered to be easily incorporated into a channel of an existing neurochip prototype. Physical dimensions of each filter and the required clock splitter are given below:

Layout Cell	Physical Dimensions
HP1F	580μm X 145μm
LP1N	470μm X 145μm
SKLP	580μm X 145μm
LPBQ	1035μm X 145μm
CLKGEN	86μm X 93μm

After passing the final design rules check and layout vs. schematic check, the layout was extracted and simulations were re-run on the extracted netlist.

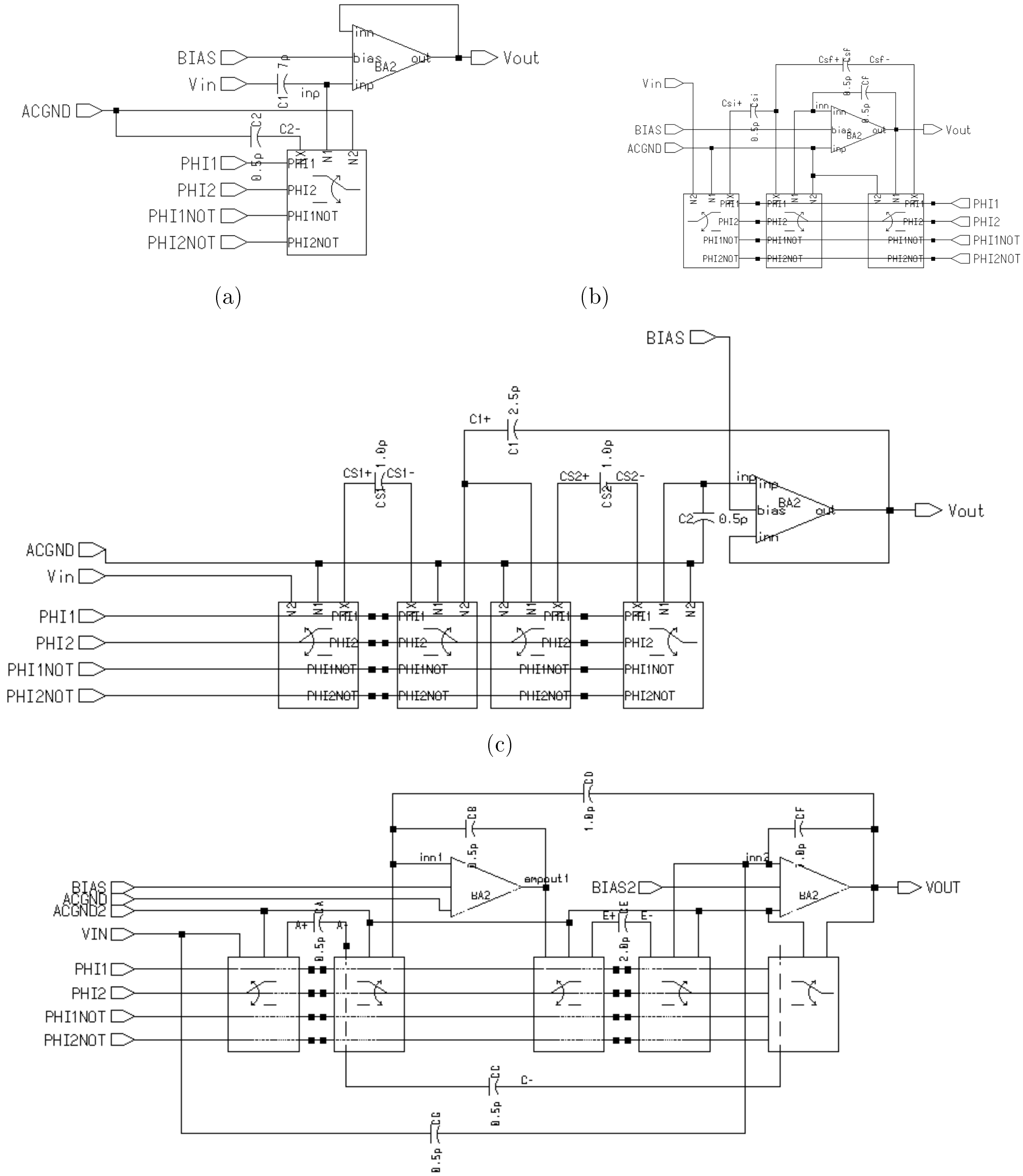

Figure 2: Schematic of a) the single-pole high-pass filter (HP1F) b) single-pole low-pass (LP1N) c) Sallen-Key low-pass filter (SKLP), and d) standard biquadratic low-pass (LPBQ)

	Passband gain [dB]	-3dB cutoff	Roll-off [dB/dec]
Single pole high pass	-1.77	501 Hz	-19.0
Single pole low pass	0.134	5.5 kHz	-11.7
Standard biquad low pass	-0.056	5.3 Hz	-35.8
Sallen-Key low pass	-4.00	5.5 kHz	-29.0

Table 1: Frequency Response Results: Gain Magnitude

3 Bench test results

The IC containing the SC filters was wire-bonded to a test chip for which a test circuit board was custom-built. All tests were run with unipolar power supplies, with ACGND set to 2.5V. Each of the four filters' inputs were tied to the same input pad to save space. Sinusoidal input signals were generated by the AudioPrecision (AP) System Two 2322 balanced analog output. A single clock signal was generated by the Agilent 33120A 15MHz function generator and was supplied via a 50-Ω coaxial cable with a 50-Ω termination to the 4-phase clock splitter. The same clock splitter's outputs fed all the filters biphasic clock inputs. All op-amps were biased with a single externally generated voltage source. Unless otherwise specified, all tests were run under the follwing input conditions:

$$
\begin{aligned}
\text{sampling clock frequency } f_{clk} &= 50.0 \text{ kHz} \\
\text{sin wave input frequency } f_{in} &= 1 \text{ kHz} \\
\text{input amplitude } \mid V_{in} \mid &= 1V_{pp} \\
\text{VDD} &= 5V \\
\text{ACGND} &= 2.5V \\
\text{GND} &= 0V \\
\text{input offset voltage } V_{OS} &= 0V \\
\text{op-amp bias voltage } V_{BIAS} &= 1.133V
\end{aligned}
$$

Frequency sweeps were performed with AP's sweep function to measure the gain magnitude response summarized in table 1. Frequency responses of cascaded filters were also tested and the outputs sum linearly as expected.

The -3dB frequencies were as accurate as 0.2% off from the targeted cutoff frequencies. Yet, tunability may prove to be a desirable feature because the bandwidth of neural signals can vary from rougly 5kHz to 10kHz. In theory, switched capacitor cutoff frequencies can be tuned by proportionally varying the clock frequency. Unfortunately, because both high pass and lowpss filters would use the same clock, the low and high cutoffs cannot be changed independently. The -3dB points were measured at different input clock frequencies and the percent change in input clock frequency $\Delta f_{clk}/f_{clk}$ was compared to the measured percent change in cutoff frequency $\Delta f_c/f_c$. results showing tunability of these cutoff frequencies are listed in table 2.

Sweeps of total harmonic distortion and noise (THD+N) across input amplitude were performed at various frequencies in the passband. THD+N improves with increasing amplitude until

$\frac{\Delta f_{clk}}{f_{clk}}$	$\frac{\Delta f_c}{f_c}$			
(in %)	HP	LP1	LPBQ	LPSK
-60.0	-59.1	-59.5	-59.7	-60.3
-20.0	-18.8	-19.6	-19.3	-20.6
+20.0	20.2	21.8	20.4	19.7
+60.0	61.7	62.5	61.5	59.4

Table 2: Sensitivity of cutoff frequency to changes in clock frequency

	Maximum SNDR [dB]			
freq [Hz]	HP	LP1	LPBQ	LPSK
1000	34.1	27.2	28.8	27.2
500		31.8	34.9	31.5
100		35.6	47.3	34.5
10		35.6	51.7	34.5

Table 3: Maximum SNDR in dB

the output begins to clip at the limits of the voltage output swing. Maximum signal-to-noise-plus-distortion ratio (SNDR) was calculated at these points of minimum THD+N, using the following formula:

$$SNDR_{max}[dB] = 20log\frac{1-N}{N}, \text{ where N is the minimum THD+N as a percent ratio}$$

To measure clock feedthrough, FFT measurements were taken with the LeCroy LT344 Waverunner oscilloscope. A pure tone both in the filter's passband (700 Hz for LP, 7 kHZ for HP) and out of band (7 kHz for LP, 700 Hz for HP) was input, and FFT magnitudes ($\hat{\mathrm{V}}$(f)) at the fundamental frequency and at the clock frequency were measured. Clock feedthrough was defined as $\hat{\mathrm{V}}(f_{clk})/\hat{\mathrm{V}}(f_{in})$

In order to estimate SNR, the noise floor was measured to be the baseline FFT magnitude with no input applied. SNR was then calculated by taking the ratio of the FFT magnitude at the fundamental frequency to the broadband baseline magnitude. Input amplitude was varied between 100 μV and the maximum input amplitude of the filter. As seen in figure 3, SNR_{dB} shows a logarithmic relationship with input amplitude and gets as high as 113 dB for HP1F and close to 100 dB for the low-pass filters at their maximum input voltages.

4 Conclusion

Four switched-capacitor filters for an implantable neural recording chip have been designed, fabricated, and tested. Low-pass filtering with a clock-tunable 5kHz corner frequency, unity passband gain, and -40dB/dec attenuation with SNDR as high as 52dB has been achieved, as well as high-pass filtering with a clock-tunable 500Hz corner frequency, -2dB passband gain, and -20dB/dec attenuation with up to 34dB of SNDR. Based on the merits of accuracy in frequency response

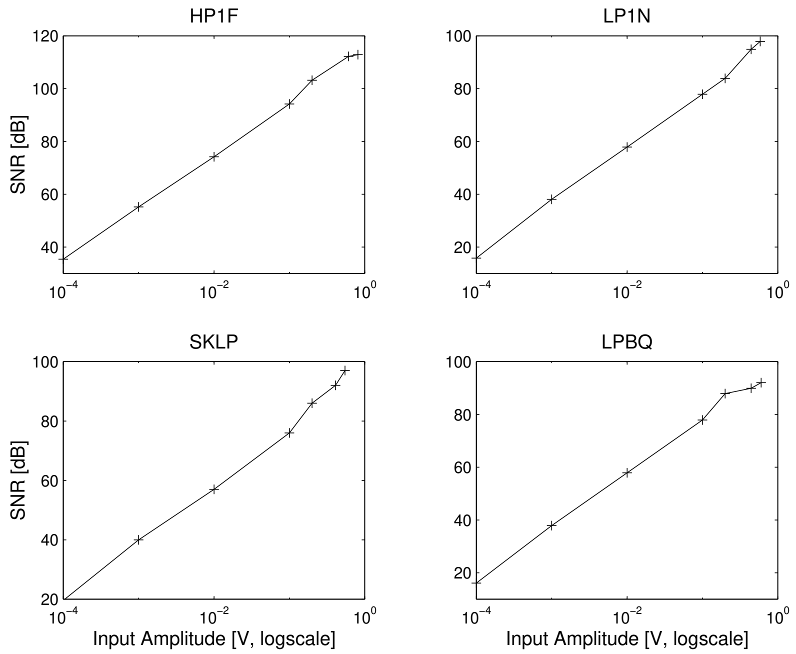

Figure 3: Signal-to-noise ratio vs. input amplitude

characteristics and best SNDR, the LPBQ would be the low-pass filter of choice for the neurochip. HP1F also meets frequency response specifications to within 5% and has a sufficient SNR and could be used in a HP1F-LPBQ cascade for the desired integrated bandpass filtering. The high pass stage will precede the low-pass stage to remove any DC offset that would take better advantage of dynamic range in following stages.

As with any sampled system, switched capacitor filters require anti-aliasing and smoothing filters. A single-pole Gm-C low-pass filter and a level-two phase shift time-constant multiplier low-pass circuit are being considered for these purposes. Currently, a 0.5pF unit-cap size is being used to prevent large relative errors due to parasitics. However, the high accuracy in the results indicate that this unit-cap can be pushed down to the technology-dependent minimum capacitor size of 0.2pF [4] to increase area-efficiency of these filters.

References

[1] Taylor, John and Huang, Quiting. in *CRC Handbook of Electrical Filters*, pp.264-271.

[2] bookamp2

[3] Gregorian, R., Martin, K., and Temes, G. "Switched-Capacitor Circuit Design," *Proc. IEEE*, vol. 71, Aug. 1983, pp. 941-986.

[4] Sansen, Willy and Peteghem, Peter. "An Area-Efficient Approach to the Design of Very-Large Time Constants in Switched-Capacitor Integrators," *IEEE J. Solid-State Circuits*, vol. SC-19, Oct. 1984, pp. 772-780.

[5] Martin, Ken and Sedra, Adel. "Exact Design of Switched-Capacitor Bandpass Filters Using Coupled-Biquad Structures," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 469-474, June 1980.